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L9: Entry 5 of 8 File: USPT Mar 8, 1994

DOCUMENT-IDENTIFIER: US 5293378 A
TITLE: Parallel multi-line packet transmission system

Abstract Text (1):
A packet transmission system wherein a packet can be transmitted at a high rate over a long transmission distance using a transmission medium which is economical and easy to handle. Under the control of a transmission controller, a separating circuit divides a packet of a packet signal into six payloads to make six transmission frames and adds a start delimiter SD and an end delimiter ED to the first and last transmission frames, and four transmitters send out the six transmission frames in accordance with sequence numbers at a rate at which the signal can be transmitted by way of time division transmission lines. Under the control of a reception controller, four receivers receive the transmission frames, and a restoring circuit assembles the transmission frames back into the original packet signal in accordance with the sequence numbers and the delimiter information.

Brief Summary Text (10):
In order to attain the object, according to the present invention, there is provided a packet transmission system, which comprises N time division transmission lines, N being an integral number equal to or greater than 2, and transmitter/receiver means for transmitting a packet signal by way of the time division transmission lines, the transmitter/receiver means including separating means for dividing a packet of the packet signal into M payloads for the packet transmission and outputting the M payloads as M transmission frames, M being an integral number equal to or greater than 2, transmitting means for coding the outputs of the separating means and transmitting them parallelly at a rate at which they can be transmitted by way of the time division transmission lines, receiving means for receiving the outputs of the transmitting means by way of the time division transmission lines and decoding the received outputs, and restoring means for assembling the outputs of the receiving means back into the original packet signal.

Brief Summary Text (11):
Preferably, the N time division transmission lines have successive sequence numbers applied thereto in advance, and the transmitting means includes means for sending out the M transmission frames into the N time division transmission lines in the order of the sequence numbers while the restoring means includes multiplexing means for assembling the M transmission frames received from the N time division transmission lines back into the original packet signal in accordance with the sequence numbers.

Brief Summary Text (15):
In the packet transmission system, the separating means of the transmitter/receiver means divides a packet of a packet signal into M payloads for the packet transmission and outputs the M payloads as M transmission frames, M being an integral number equal to or greater than 2. The transmitting means codes the outputs of the separating means and transmits them parallelly at a rate at which they can be transmitted by way of the N time division transmission lines, N being an integral number equal to or greater than 2. The receiving means receives the outputs of the transmitting means by way of the N time division transmission lines and decodes the received outputs. The restoring means multiplexes the outputs of the receiving means back into the original packet signal.

Detailed Description Text (3):
The transmitter/receiver means includes a transmission buffer 1, a separating circuit 11 connected to the transmission buffer 1, four registers 12 to 15 connected to the separating circuit 11, four transmitters 16 to 19 connected to the registers 12 to 15, respectively, a transmission controller 10 connected to the transmission buffer 1, separating circuit 11 and transmitters 16 to 19, four receivers 26 to 29 connected to

the transmitters 16 to 19 by way of the time division transmission lines 5 to 8, respectively, four registers 22 to 25 connected to the receivers 26 to 29, respectively, a restoring circuit 21 connected to the registers 22 to 25, a reception buffer 2 connected to the restoring circuit 21, and a reception controller 20 connected to the receivers 26 to 29, restoring circuit 21 and reception buffer 2.

Detailed Description Text (4):
The transmission buffer 1, the separating circuit 11, the registers 12 to 15 and part of the transmission controller 10 serve as separating means for separating a packet of a packet signal into six payloads for the packet transfer and outputting them as six transmission frames; the transmitters 16 to 19 and part of the transmission controller 10 serve as transmitting means for coding the outputs of the registers 12 to 15 and transmitting them parallelly at a rate at which they can be transmitted by way of the time division transmission lines 5 to 8; the receivers 26 to 29 and part of the reception controller 20 serve as receiving means for receiving the outputs of the transmitters 16 to 19 by way of the time division transmission lines 5 to 8, respectively, and decoding them; and the registers 22 to 25, the restoring circuit 21, the reception buffer 2 and part of the reception controller 20 serve as restoring means for assembling the outputs of the receivers 26 to 29 back into an original packet signal.

Detailed Description Text (5):
Sequence numbers are applied in advance to the time division transmission lines 5 to 8, and the transmitters 16 to 19 include means for sending out transmission frames in the order of the sequence numbers into the time division transmission lines 5 to 8 under the control of the transmission controller 10. Meanwhile, the restoring circuit 21 includes means for assembling the six transmission frames received from the time division transmission lines 5 to 8 back into an original packet signal in accordance with the sequence numbers under the control of the reception controller 20.

Detailed Description Text (6):
Further, the separating circuit 11 includes means for adding a delimiter field for the transmission of delimiter information to a predetermined transmission frame under the control of the transmission controller 10. Meanwhile, the restoring circuit 21 includes means for assembling the six transfer frames received from the time division transmission lines 5 to 8 back into an original packet signal in accordance with the sequence numbers and the delimiter information of the delimiter field under the control of the reception controller 20.

Detailed Description Text (8):
Operation of the packet transmission system of the construction when a start delimiter and an end delimiter are used for a transmission frame is described with reference to FIG. 2. A packet signal includes a destination address DA, a source address SA, information INFO and a frame check sequence FCS. A packet signal frame 100 is delimited by a start delimiter SD and an end delimiter ED. The packet signal in the transmission buffer 1 is divided by way of the separating circuit 11 under the control of the transmission controller 10 into six segments a to f, which are supplied to the registers 12 to 15 in this order. Thus, transmission frames 101 to 104 are supplied into the transmission lines 5 to 8. Synchronizing signals SYN are added to each of the transmission frames 101 to 104. The start delimiter SD is applied to the transmission frame 101 for carrying the first segment a of the packet signal by a transmission code violation (intentional violation of a transmission coding rule). The segments b to d are transmitted by way of the transmission lines 6 to 8, respectively, and the segments e and f are transmitted in the next frame cycle. The end delimiter ED is applied after the last segment f by the transmission coding violation. The transmission code violation can be provided peculiarly to the transmission code. When, for example, the AMI code is employed, while it is a coding rule of the AMI code that "+1" and "-1" are provided alternately to a binary digital signal each time "1" appears in the binary digital signal, the transmission code train of, for example, "0", "+1", "0", "+1", "0", "-1", "0" and "-1" is provided as the start delimiter SD, and the transmission code train of, for example, "0", "-1", "0", "-1", "0", "+1", "0" and "+1" is provided as the end delimiter ED. It is to be noted that they are a mere example and do not limit the scope of the present invention.

Detailed Description Text (9):
The transmission controller 10 performs the following control. When the transmission controller 10 detects arrival of a packet signal at the transmission buffer 1, it adds the word "01010101" corresponding to the start delimiter SD and the end delimiter ED to the packet signal. Then, it divides the packet signal with the length of a payload of a

time division frame and writes the thus divided segments into the registers 12 to 15 by way of the separating circuit 11. The transmitters 16 to 19 code the binary digital signals of the segments stored in the registers 12 to 15, respectively, into transmission codes and send out the transmission codes to the transmission lines 5 to 8, respectively. The communication controller 10 effects control of the transmitters 16 to 19 so that such a coding violation as described above by way of the example may be provided to the words of the start delimiter SD and the end delimiter ED.

Detailed Description Text (10):
Subsequently, operation on the receiver side is described. Frame synchronization of the individual transmission lines 5 to 8 is maintained at the receivers 26 to 29, respectively, and detection of the start delimiter SD and the end delimiter ED is effected by monitoring a transmission code violation. The thus detected start delimiter SD and end delimiter ED are notified to the reception controller 20. Signals decoded into binary digital signals by the receivers 26 to 29 are written once into the registers 22 to 25, respectively, and then restored into the original packet signal by the restoring circuit 21. The thus restored original packet signal is subsequently stored into the reception buffer 2. In this instance, the reception controller 20 controls, in response to the detected start delimiter SD and end delimiter ED, the restoring circuit 21 in accordance with the order of the transmission lines 5 to 8 and writes the time division frame 100 of the packet signal shown in FIG. 2 into the reception buffer 2.

Detailed Description Text (12):
On the receiver side, the signal BOF is decoded by the corresponding receiver 27, and it is notified to the reception controller 20 that the signal BOF is "1". The reception controller 20 thus detects starting of transmission of a packet signal and then reads out packet length information LENGTH in the packet signal. Segment information stored in the registers 22 to 25 is restored into the original packet signal by the restoring circuit 21 and stored into the reception buffer 2. An end of the packet signal is specified by the length information LENGTH read out as above. It is to be noted that packet length information LENGTH to be newly added need not be added to the head of a packet signal and may be added at a fixed position in a packet signal. Further, in case length information is provided in advance to a packet signal, there is no need of newly adding length information to the packet signal but the original length information may be used.

CLAIMS:

1. A parallel multi-line packet transmission system, comprising:

N time division transmission lines, N being an integral number equal to or greater than 2, which have successive sequence numbers applied thereto in advance; and

transmitter/receiver means for transmitting a packet signal by way of said time division transmission lines, said transmitter/receiver means including:

separating means for dividing a packet of the packet signal into M payloads for the packet transmission and outputting the M payloads as M transmission frames, M being an integral number equal to or greater than 2;

transmitting means for adding packet length information to the original packet signal as a delimiter information, adding to each of said M transmission frames a signal representing whether or not transmission of said packet signal is started in the transmission frame, coding the outputs of said separating means, transmitting them parallelly at a predetermined rate by way of said time division transmission lines, and sending out M transmission frames into the N time division transmission lines in order of the sequence numbers;

receiving means for receiving the outputs of said transmitting means by way of said time division transmission lines and decoding the received outputs; and

restoring means for assembling the M transmission frames received from said N time division transmission lines back into the original packet signal in accordance with the sequence numbers.

2. A parallel multi-line packet transmission system as claimed in claim 1, wherein said restoring means includes multiplexing means for assembling the M transmission frames received from said N time division transmission lines back into the original packet

signal in accordance with the sequence numbers.

6. A parallel multi-line packet transmission system, comprising:

N time division transmission lines, N being an integral number equal to or greater than 2; which have successive sequence numbers applied thereto in advance; and

transmitter/receiver means for transmitting a packet signal by way of said time division transmission lines, said transmitter/receiver means including:

separating means for dividing a packet of the packet signal into payloads for the packet transmission and outputting the payloads as M transmission frames, M being an integral number equal to or greater than 2;

transmitting means for coding the outputs of said separating means and transmitting them parallelly at a predetermined rate by way of said time division transmission lines;

receiving means for receiving the outputs of said transmitting means by way of said time division transmission lines and decoding the received outputs; and

restoring means for assembling the output of said receiving means back into the original packet signal,

wherein each of the M transmission frames includes a plurality of subframes each including a payload.

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L4: Entry 1 of 9 File: USPT Apr 29, 2003

DOCUMENT-IDENTIFIER: US 6556539 B1
TITLE: Selector switch control using priority table

Detailed Description Text (76):
Although described below in the context of network synchronization management, it would be apparent to those skilled in the art that the management functions and performance metrics are applicable to management of a telecommunications network in general. For example, diversity considerations can be used in any network requiring alternate destination paths to improve the robustness of the network's ability to restore itself. Likewise, the Q-metric can be used to calculate a particular path's communications quality in any network model. In the context of network synchronization management, a communication signal is a synchronization signal or timing signal.

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L4: Entry 8 of 9 File: USPT Feb 27, 1996

DOCUMENT-IDENTIFIER: US 5495471 A
TITLE: System and method for restoring a telecommunications network based on a two prong approach

Detailed Description Text (40):
Performance metrics 1 and 2, when combined, are the most critical performance criteria for any network restoration algorithm. The ideal is a 100% restoration within two seconds. In situations in which an algorithm cannot achieve full restoration within two seconds, the rate at which the algorithm restores lost channels can be important. FIG. 8 illustrates this point. The vertical axis represents level of restoration and the horizontal axis the time required to achieve that level of restoration. The two curves represent the rate at which two algorithms, 1 and 2, achieve increasing levels of restoration. Three time marks, A, B, and C, are shown. If two seconds of elapsed time occurs at time mark C, then both algorithms have restored 100%. If, however, two seconds of elapsed time occurs at time mark A, then algorithm 1 is clearly superior to algorithm 2 as it achieves a higher level of restoration. On the other hand, if two seconds of elapsed time occurs at time mark B, then the restoration level achieved by algorithm 2 is higher than algorithm 1.

Detailed Description Text (42):
The range of application performance metric refers to what different kinds of failure scenarios the algorithm can be applied to affect restoration. A number of the proposed distributed algorithms can only address single link failures. A limited number of algorithms can be used to restore lost working channels in multiple link failure and node failure scenarios.

Detailed Description Text (43):
The message volume performance metric refers to how many network restoration messages are generated by a restoration algorithm. It is desirable that the number of messages an algorithm generates be as few as possible. Not only does message volume affect performance metric 1 (time to restore), it also limits other network restoration message traffic flow during the restoration process which may be of high or critical priority.

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L9: Entry 2 of 8 File: USPT Mar 6, 2001

DOCUMENT-IDENTIFIER: US 6198413 B1
TITLE: Partitioned DC balanced (0,6) 16B/18B transmission code with error correction

Brief Summary Text (8):
The high gain fiber optic receivers need an ac coupling stage near the front end. The control of the drive level, receiver gain, and equalization is simplified and the precision of control is improved, if it can be based on the average signal power, especially at top rates. DC restore circuits tend to lose precision with rising data rates and cease to operate properly below the maximum rates for other circuits required in a transceiver. Finally, if the time constants associated with the parasitic capacitances at the front end of a receiver are comparable to or longer than a baud interval, a signal with reduced low frequency content will suffer less distortion and will enable many links to operate without an equalizing circuit.

Brief Summary Text (18):
U.S. Pat. No. 5,740,186 to Widmer, entitled "Apparatus and Method for Error Correction Based on Transmission Code Violations and Parity," the disclosure of which is incorporated herein by reference, discloses techniques for correcting errors in binary transmission coded data.

Detailed Description Text (46):
Referring now to FIG. 5, a block diagram of an exemplary decoder 5000 for implementing a 16B/18B transmission code according to the invention is shown. It is to be appreciated that FIG. 5 illustrates an overall functional organization of an 18B/16B decoder of the present invention. Accordingly, FIG. 5 also represents in essence a data flow chart for the decoding system. The decoder 5000 includes a 10B/9B decoder 5002, an 8B/7B decoder 5004, and a disparity checks unit 5006. The decoder circuit includes code violation and disparity error checks. In the presence of errors, the received blocks may have a disparity of 6, 8 or 10, which may be lumped together with the disparity of 4 for the purposes of the running disparity (+4, -4). It is to be understood that an 18B/16B decoder according to the invention may be implemented in accordance with one or more of the approaches mentioned above for the 16B/18B encoder. However, other implementation approaches may be employed.

Detailed Description Text (49):
As previously mentioned, the 16B/18B transmission coding system of the invention preferably implements an error correction methodology. In one embodiment, error correction according to the present invention is implemented in a manner that modifies aspects of the techniques disclosed in U.S. Pat. No. 5,740,186 ('186 patent) to Widmer, entitled "Apparatus and Method for Error Correction Based on Transmission Code Violations and Parity," the disclosure of which is incorporated herein by reference. The '186 patent discloses techniques for correcting errors in 8B/10B binary transmission coded data employed in accordance with the Fibre Channel Standard (FCS). Accordingly, a description of the '186 patent error correction technique is provided below followed by the inventive modifications to the techniques for use with the 16B/18B transmission code of the invention.

Detailed Description Text (54):
For the Fibre Channel Standard (FCS) transmission code, it has been calculated that statistically an error is with high probability within 16 bytes preceding the identified disparity violation for the case of random data. The probability that the error is more than 16 bytes preceding the disparity violation is about 2.times.10.sup.-9. As described above, the balance parities identify the location of the byte having the error and the vertical parity identifies the location of the particular bits having errors. The procedure described above using a vertical parity and a new balance parity is used with codes which do not contain local parity.

Therefore, the procedure described above supplements codes which do not have local parity.

Detailed Description Text (57):
When using FCS transmission code violations for error locating, Balance Bits BB and QB are defined for each coded byte and 4-byte word, respectively, with a value of one for balanced blocks and zero otherwise. Sets of 4 BB and 4 QB bits are each arranged diagonally in separate quadruplets for successive groups of 4 bytes and 4 words, respectively. A parity bit is derived for each of the diagonal bit positions of all the BB and the QB sets of a frame. Only these 8 parity bits BPAR (refers to balance parity 254) are transmitted after the end of the frame. For random data, the FCS code by itself locates all single byte errors to a range of 16 bytes except one error in 5.times.10.sup.8 errors. Violations in the received BPAR bits are used to trace an error more precisely to a specific byte of the 16 byte group identified by the code. A set VPAR (refers to vertical parity 258) of 8 vertical parity bits derived from the uncoded data, and the 8 BPAR bits are coded and packed into the first Idle word following the End of Frame. After identification of a faulty byte at the receiver, the VPAR bits are used to correct it.

Detailed Description Text (65):
In the commonly used parity matrix, the horizontal parity is an explicit bit for each matrix line. In the example below, the horizontal parity is instead supplied by the combination of a transmission code and a few parity bits at the end of the frame, computed on features of the code which are guaranteed to change for an odd number of errors. Transmission codes are subject to several constraints to enhance reliable low cost transmission. Additional constraints can be built into a code, so any odd number of errors in a byte or word generates an invalid word. Such a property of the code is referred to as "local parity." For general applications, such codes are less desirable, because the added constraint makes it necessary to degrade some transmission parameters, and to accept a more complex and higher cost implementation. Other 8B/10B codes, including the FCS Standard code, most times also indicate immediately an invalid byte when an error has occurred. However, a substantial ratio of errors generates only a disparity violation farther down the bit stream, away from the byte where the error occurred, and so the byte which contains the error(s) cannot directly be identified.

Detailed Description Text (71):
Lets say an error occurred in a byte with the binary address 0.sub.-- 1110 and did not generate a code violation at that point, but only a disparity violation 3 bytes later at address 1.sub.-- 0001. In the receiver, the address 1.sub.-- 0001 is recorded. At the end of the frame, PB2 will be in violation and thus indicates that the error occurred in a byte with low order binary address 10. The assumption is that the error was in the set of 4 bytes ending with the transmission code violation at address 1.sub.-- 0001. Reducing this address in steps by one until the two low order bits match 10 results in the address 0.sub.-- 1110, the actual location of the error.

Detailed Description Text (73):
An error will cause a transmission code violation which points to a set of 16 consecutive bytes likely to contain the error. A parity violation in a PQy bit identifies the specific erroneous word from the set of 4 words flagged by the code, and a violation in a PBx bit points to a particular byte in that word. The function of the PQy and PBx quadruplets is solely to enhance the error locating capabilities of the FC transmission code, not to correct the error.

Detailed Description Text (133):
In a system, error correction may be done strictly on a per link basis, i.e. between a single transmitter and receiver, or end to end, which may include several links and switches. In the first case, this proposal can be made invisible to the higher levels of the architecture. The transmitter simply modifies the last 3 bytes of the first Idle after EOF. At the receiver, the error correction circuitry connects to the de-serializer and the decoder. It corrects the frames before passing them on to the next level, and it restores the first Idle word. For this approach it does not matter how the switch handles the Idles.

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L9: Entry 3 of 8 File: USPT Jul 21, 1998

DOCUMENT-IDENTIFIER: US 5784387 A
TITLE: Method for detecting start-of-frame, end of frame and idle words in a data stream

Brief Summary Text (17):
The raw binary data is generally not transmitted but is first converted into coded data having bytes with a larger number of bits than contained in the raw data bytes. Coding is used for a number of reasons. A delimiter is needed to define word boundaries and frame boundaries. A delimiter is needed to that when data is transmitted, the receiver can determine where the frame of data which is being sent begins. The delimiter is commonly referred to as a comma. Also, it is desirable when transmitting data to have run lengths of consecutive ones or of consecutive zeros which are short in order to provide a steady stream of transitions as timing references to the clock recovery circuit of the receiver. Coded data is used to limit the run length to less than some predetermined value. Also, it is desirable to have data which is DC balanced to the extent that the digital sum variation over any number of consecutive bits is finite and small. If there are a large number of ones or zeros consecutively, the charge levels on reactive components will increase, adversely affecting AC coupling by requiring longer time constants or automatic level restore circuits.

Brief Summary Text (19):
It is an object of the present invention to provide an improved horizontal parity technique for identifying the location of errors in coded bytes wherein the code does not have local parity and wherein transmission code violations in combination with a limited set (e.g. 8) of parity bits computed from a parameter of each coded byte can locate the error location to a particular byte.

Detailed Description Text (1):
Table I illustrates error location with 2 levels of balance bits and Fibre Channel Standard transmission code violations.

Detailed Description Text (9):
For the Fibre Channel Standard transmission code, it has been calculated that statistically an error is with high probability within 16 bytes proceding the identified disparity violation for the case of random data. The probability that the error is more than 16 bytes preceding the disparity violation is about 2.times.10.sup.9. As described above, the balance parities identify the location of the byte having the error and the vertical parity identifies the location of the particular bits having errors. The procedure described above using a vertical parity and a new balance parity, according to the present invention, is used with codes which do not contain local parity. Therefore, the procedure described above supplements codes which do not have local parity. The FCS code as described by Widmer [1983] does not have local parity and, therefore, the ability to identify errors is supplemented by the procedure described above according to the present invention.

Detailed Description Text (12):
When using FCS transmission code violations for error locating. Balance Bits BB and BQ are defined for each coded byte and 4-byte word, respectively, with a value of one for balanced blocks and zero otherwise. Sets of 4 BB and 4 BQ bits are each arranged diagonally in separate quadruplets for successive groups of 4 bytes and 4 words, respectively. A parity bit is derived for each of the diagonal bit positions of all the BB and the BQ sets of a frame. Only these 8 parity bits BPAR are transmitted after the end of the frame. For random data, the FCS code by itself locates all single byte errors to a range of 16 bytes except one error in 5.times.10.sup.8 errors. Violations in the received BPAR bits are used to trace an error more precisely to a specific byte of the 16 byte group identified by the code. A set VPAR of 8 vertical parity bits

derived from the uncoded data, and the 8 BPAR bits are coded and packed into the first Idle word following the End of Frame. After identification of a faulty byte at the receiver, the VPAR bits are used to correct it.

Detailed Description Text (21):
In the example below, the horizontal parity is instead supplied by the combination of a transmission code and a few parity bits at the end of the frame, computed on features of the code which are guaranteed to change for an odd number of errors. Transmission codes are subject to several constraints to enhance reliable low cost transmission. Additional constraints can be built into a code, so any odd number of errors in a byte or word generates an invalid word. Such a property of the code is referred to as `local parity` [Martin, 1985]. For general applications, such codes are less desirable, because the added constraint makes it necessary to degrade some transmission parameters, and to accept a more complex and higher cost implementation. Other 8B/10B codes, including the FCS Standard code, most times also indicate immediately an invalid byte when an error has occurred. However, a substantial ratio of errors generates only a disparity violation farther down the bit stream, away from the byte where the error occurred, and so the byte which contains the error(s) cannot directly be identified.

Detailed Description Text (28):
Lets say an error occurred in a byte with the binary address `0.sub.13 1110` and did not generate a code violation at that point, but only a disparity violation 3 bytes later at address `1.sub.-- 0001`. In the receiver, the address `1.sub.13 0001` is recorded. At the end of the frame, PB2 will in violation and thus indicates that the error occurred in a byte with low order binary address `10`. The assumption is that the error was in the set of 4 bytes ending with the transmission code violation at address `1.sub.-- 0001`. Reducing this address in steps by one until the two low order bits match `10` results in the address `0.sub.-- 1110`, the actual location of the error.

Detailed Description Text (30):
An error will cause a transmission code violation which points to a set of 16 consecutive bytes likely to contain the error. A parity violation in a PQy bit identifies the specific erroneous word from the set of 4 words flagged by the code, and a violation in a PBx bit points to a particular byte in that word. The function of the PQy and PBx quadruplets is solely to enhance the error locating capabilities of the FC transmission code, not to correct the error.

Detailed Description Text (34):
If the first violation is a disparity violation rather than an outright invalid byte, the location of the faulty byte must first be determined with the help of the parity violations of the balance bits PQy and PBx as described under "Horizontal Parity with Fibre Channel Standard Transmission Code" above. Then correction is done as above. Correction is suspended, if the disparity violation is followed by an invalid byte or by more than one other disparity violation, which all indicate multiple errors in different bytes.

Detailed Description Text (86):
In a system, error correction may be done strictly on a per link basis, i.e. between a single transmitter and receiver, or end to end, which may include several links and switches. In the first case, this proposal can be made invisible to the higher levels of the architecture. The transmitter simply modifies the last 3 bytes of the first Idle after EOF. At the receiver, the error correction circuitry connects to the deserializer and the decoder. It corrects the frames before passing them on the next level, and it restores the first Idle word. For this approach it does not matter how the switch handles the Idles.